IN THE SPECIFICATION:

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] Discrete testing includes testing the semiconductor dice for speed and for errors which may occur after fabrication and after burn-in. Burn-in is a reliability test of a semiconductor die to identify physical and electrical defects ~~which~~ that would cause the semiconductor die to fail to perform to specifications or to fail altogether before its normal operational life cycle is reached. Thus, the semiconductor die is subjected to an initial heavy duty cycle ~~which~~ that elicits latent silicon defects. Burn-in testing is usually conducted at elevated potentials and for a prolonged period of time, typically 24 hours, at varying and reduced and elevated temperatures, such as -15°C to 125°C, to accelerate failure mechanisms. Semiconductor dice ~~which~~ that survive discrete testing and burn-in are termed "known good die," or "KGD."

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Such flip-chips may be tested and/or burned-in prior to their permanent connection to a carrier substrate by placing each flip-chip in a temporary package, such as those discussed above. As shown in FIG. 31, each solder ball 304 attached to a bond pad 302 of a flip-chip-configured die 300 is in physical contact with a conductive trace 306 on a contact wall 308 of the temporary package. The conductive traces 306 transmit electrical signals to the die 300 for testing or burn-in. With such a temporary package, each solder ball 304 contacts each conductive trace 306 at only one contact point 310. With only one contact point 310 per solder ball 304, all of the stresses caused by biasing the die 300 to the contact wall 308 of the temporary package are concentrated on the one contact point 310 on each solder ball 304. These stresses can result in the solder balls 304 fracturing, dislodging from the bond pad 302, or otherwise damaging the flip-chip-configured die 300.

Please replace paragraph number **[0010]** with the following rewritten paragraph:

[0010] Furthermore, such a temporary package configuration is also insensitive to ensuring electrical connection to the temporary package of non-spherical/irregularly shaped solder balls, or different sized balls, in the BGA. FIG. 32 illustrates an ~~under~~under-sized solder ball 312 in the arrangement similar to that shown in FIG. 31. Elements common between FIG. 31 and FIG. 32 retain the same designation. The ~~under~~under-sized solder ball 312 does not make contact with the conductive trace 306. This can give a false failure indication for the die, when, in reality, it could be "good" when an adequate connection is achieved when the undersized ball 312 is refluxed for permanent attachment to a carrier substrate. At the least, the die in question is initially rejected and must be retested to verify the source of the apparent failure.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] In one embodiment of the invention, multiple passivation and trace layers are employed to accommodate small-pitched connection element arrays having as many as a thousand or more inputs and outputs ~~("I/Os").~~ (I/Os).

Please replace paragraph number **[0021]** with the following rewritten paragraph:

[0021] FIG. 11 illustrates an ~~under~~under-sized solder ball and a misshapen solder ball of a die on a substrate, such as a silicon test package insert, residing in interconnections of the present invention;

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] FIGS. 1-9 illustrate side cross-sectional views of a method of forming a single interconnection of the present invention, although typically hundreds, if not thousands, of such interconnections may be simultaneously fabricated on a single substrate. It should be understood that the figures presented in conjunction with this description are not meant to be illustrations of actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized ~~representations~~ representations, which are employed to more clearly and fully

depict the process of the invention than would otherwise be possible. It should also be understood that the figures herein are not meant to be to scale nor otherwise in specific proportion, nor should they be so taken.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] FIG. 1 illustrates a conductive trace 104, preferably of copper, formed on a dielectric layer 102 (preferably thermally grown ~~SiO_2)~~ SiO_2), which resides on a semiconductor substrate, such as a silicon wafer 100. A bulk silicon structure, such as a silicon-on-sapphire (SOS) structure, a silicon-on-glass (SOG) structure, or other silicon-on-insulator (SOI) structure, may also be employed. By employing silicon at least as the exposed substrate layer supporting interconnections according to the invention, the coefficient of thermal expansion (CTE) is matched with that of the silicon semiconductor die, partial wafer or wafer under test, a significant feature given the wide temperature swings experienced by the die and substrate bearing the inventive interconnections during burn-in. Thus, thermally-induced stresses on the solder balls of a flip-chip configured die, partial wafer or wafer are minimized.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] The conductive trace 104 contacts external circuitry of the package base (not shown) through TAB tape, wire bonds, or other conductive structures, which transmit appropriate electrical signals for burn-in, testing, or the like. A passivation film 106 is formed over the dielectric layer 102, as well as the conductive trace 104, as shown in FIG. 2. The passivation film 106 is preferably a polyimide film or other thick resin with a thickness of about 0.8 ~~to1~~ to 1 mil, or ~~20-25~~ 20 to 25 microns, if a nominal 3 mil, or 75 micron, solder ball is to be contacted, as will be explained below. If the ball size is enlarged, for example, to about 13 mil or 325 microns, then the thickness of this film should be changed accordingly to about 4 mil, or 100 microns. While other passivation materials such as silicon nitride, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG) or borosilicate glass (BSG) may be employed, polyimide is preferred as it exhibits a lower ε than the other materials, resulting in reduced capacitance in the ~~structure~~ structure, including the interconnection and associated ~~traces,~~ traces

and faster signal transmission along the copper insert traces. A layer of etchant-resistive photoresist film 108 is then applied over the passivation film 106, as shown in FIG. 3. The photoresist film 108 is then masked, exposed, and stripped to form a desired opening 112, preferably circular, in the photoresist film 108, as shown in FIG. 4. The passivation film 106 is then etched through the opening 112 in photoresist film ~~08~~ 108 to form a via 114 with either sloped edges or walls 118 (preferably by facet etching) or straight (vertical) walls if desired, and which exposes a face surface 116 of the conductive trace 104, as shown in FIG. 5. The photoresist film 108 is then stripped, as shown in FIG. 6.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] A layer of etchant-resistive photoresist film is applied over metal layer 120 and is then masked, exposed, and stripped to form an etchant-resistive block 122 over the via 114, as shown in FIG. 8. The metal layer 120 surrounding the via 114 is then etched down to the surface of passivation film 106 and the etchant-resistive block 122 is stripped to form a discrete interconnection 124, as shown in FIG. 9. The discrete interconnection 124, for example, receives a solder ball 126 (typically a 95%:5% or 63%:37% lead/tin solder ~~ball)~~ ball), which is attached to a bond pad 130 of a semiconductor element 128, such as a die, partial wafer or wafer, as shown in FIG. 10. The discrete interconnection 124 is sized in combination with the slope of the walls of the sloped-wall ~~via~~ via 114 as shown and the depth or thickness of the passivation film 106 through which via 114 is etched to receive therein approximately 10% to 50%, and preferably about 30%, of the overall height of the solder ball 126. In other words, the height 132 within the discrete interconnection 124 is approximately 10% to 50%, and preferably about 30%, of the overall height 134 of the solder ball 126. The solder ball 126 preferably makes contact with the discrete interconnection 124 at a contact line 136 at least partially circling the solder ball 126. The shape of the discrete interconnection 124 allows ~~under~~under-sized solder balls 138 and misshapen solder balls 140, which are attached to bond pads 130 of semiconductor element 128, to still make adequate electrical contact with the discrete interconnection 124, as shown in FIG. 11. Moreover, thermally-induced fatigue, which can result in solder ball breakage, is lessened due to the enhanced contact area.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] FIGS. 12-25 illustrate an alternative method of forming an interconnection of the present invention. FIG. 12 illustrates a conductive trace 146 (again, preferably of copper) formed on a dielectric layer 144 (again, preferably of a thermally grown ~~oxide)~~ oxide), which resides on a semiconductor substrate 142. The conductive trace 146 contacts external circuitry (not shown) ~~which~~ that transmits appropriate electrical signals for burn-in, testing, or the like. A passivation film 148, preferably a polyimide film, is formed over the dielectric layer 144, as well as the conductive trace 146, as shown in FIG. 13. A layer of etchant-resistive photoresist film 150 is then applied over the passivation film 148 and is then masked, exposed, and stripped to form a desired opening 152, preferably circular, in the photoresist film 150, as shown in FIG. 14. The passivation film 148 is then etched through the opening 152 in photoresist film 150 to a predetermined depth to form a first via portion 154 into the passivation film 148, as shown in FIG. 15. A first layer of silicon dioxide 156 is deposited over the photoresist film 150 and an exposed portion of the passivation film 148, as shown in FIG. 16. The first layer of silicon dioxide ~~layer~~ 156 is then etched, preferably spacer etched, to form a first lip 158 of silicon dioxide in the corners 160 of the first via portion 154 and to expose a portion of the passivation film 148 in the first via portion 154, as shown in FIG. 17.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] As shown in FIG. 18, the passivation film 148 is again etched to a predetermined depth to form a second via portion 162. A second layer of silicon dioxide 164 is deposited over the photoresist film 150, the first lip 158, and an exposed portion of the passivation film 148, as shown in FIG. 19. The second layer of silicon dioxide ~~layer~~ 164 is then etched to form a second lip 166 of silicon dioxide in the corners 168 of the second via portion 162 and to expose a portion of the passivation film 148 in the second via portion 162, as shown in FIG. 20. The passivation film 148 is again etched to a predetermined depth to form a third via portion 170, as shown in FIG. 21.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] The discrete interconnection 178 has a staggered ~~surface~~ surface, which may contact the solder ball 180 at several contact lines 192 circling or partially circling the solder ball 180. The shape of the discrete interconnection 178 allows small solder balls 194 and misshapen solder balls 196, which are attached to bond pads 184 of semiconductor element 186, to still make extensive electrical contact with the discrete interconnection 178, as shown in FIG. 27.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] It is, of course, understood that the conductive traces such as 104, 146 need not necessarily be buried under the passivation film 106, 148. FIG. 28 shows an alternate conductive trace configuration 200. The alternate conductive trace configuration 200 comprises a substrate 202 with a passivation film 206 formed over a dielectric layer 204. A ~~via~~ via 207 is formed in the passivation film 206 as discussed above. The conductive trace 208 is then formed over the passivation film 206 and into the ~~via.~~ via 207. A discrete interconnection 210, such as a layer of gold or other oxidation-resistant metal, is formed on the portion of conductive trace 208 lying within the ~~via.~~ via 207.